HOLT INC.
INTEGRATED CIRCUITS

HI-8596

June 2024

Single-Rail ARINC 429 Differential Line Driver

GENERAL DESCRIPTION

The HI-8596 bus interface product is a silicon gate CMOS device designed as a line driver in accordance with the ARINC 429 bus specifications. The part includes a dual polarity voltage doubler, allowing it to operate from a single +3.3V supply using only four external capacitors. The part also features high-impedance outputs (tri-state) when both data inputs are taken high, allowing multiple line drivers to be connected to a common bus.

Logic inputs feature built-in 4kV ESD input protection (HBM) as well as 5V or 3.3V logic level compatibility.

37.5 Ohm or 5 Ohm resistors in series with each ARINC output are available to allow the use of external resistors for lightning protection.

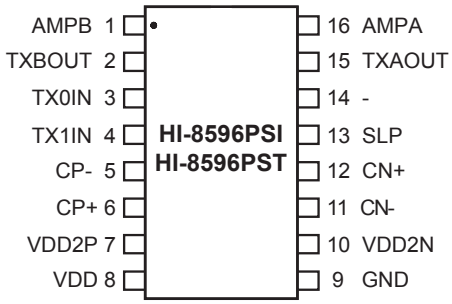
The HI-8596 line driver is intended for use where logic signals must be converted to ARINC 429 levels such as when using an FPGA or the HI-3586 ARINC 429 protocol IC.

The part is available in Industrial -40°C to +85°C, or Extended, -55°C to +125°C temperature ranges. Optional burn-in is available on the extended temperature range.

FEATURES

- Single +3.3V supply
- All ARINC 429 voltage levels generated on-chip
- Digitally selectable rise and fall times
- Tri-state Outputs
- 5 Ohm or 37.5 Ohm output resistance
- Industrial and Extended temperature ranges
- Burn-in available

PIN CONFIGURATION (TOP VIEW)



16-Pin Plastic SOIC package (Narrow Body)

(*See page 9 for additional package pin configurations*)

Table 1. Function Table

TX1IN	TX0IN	SLP	TXAOUT	TXBOUT	SLOPE
0	0	X	0V	0V	N/A
0	1	0	-5V	5V	10µs
0	1	1	-5V	5V	1.5µs
1	0	0	5V	-5V	10µs
1	0	1	5V	-5V	1.5µs
1	1	X	Hi-Z	Hi-Z	N/A

BLOCK DIAGRAM

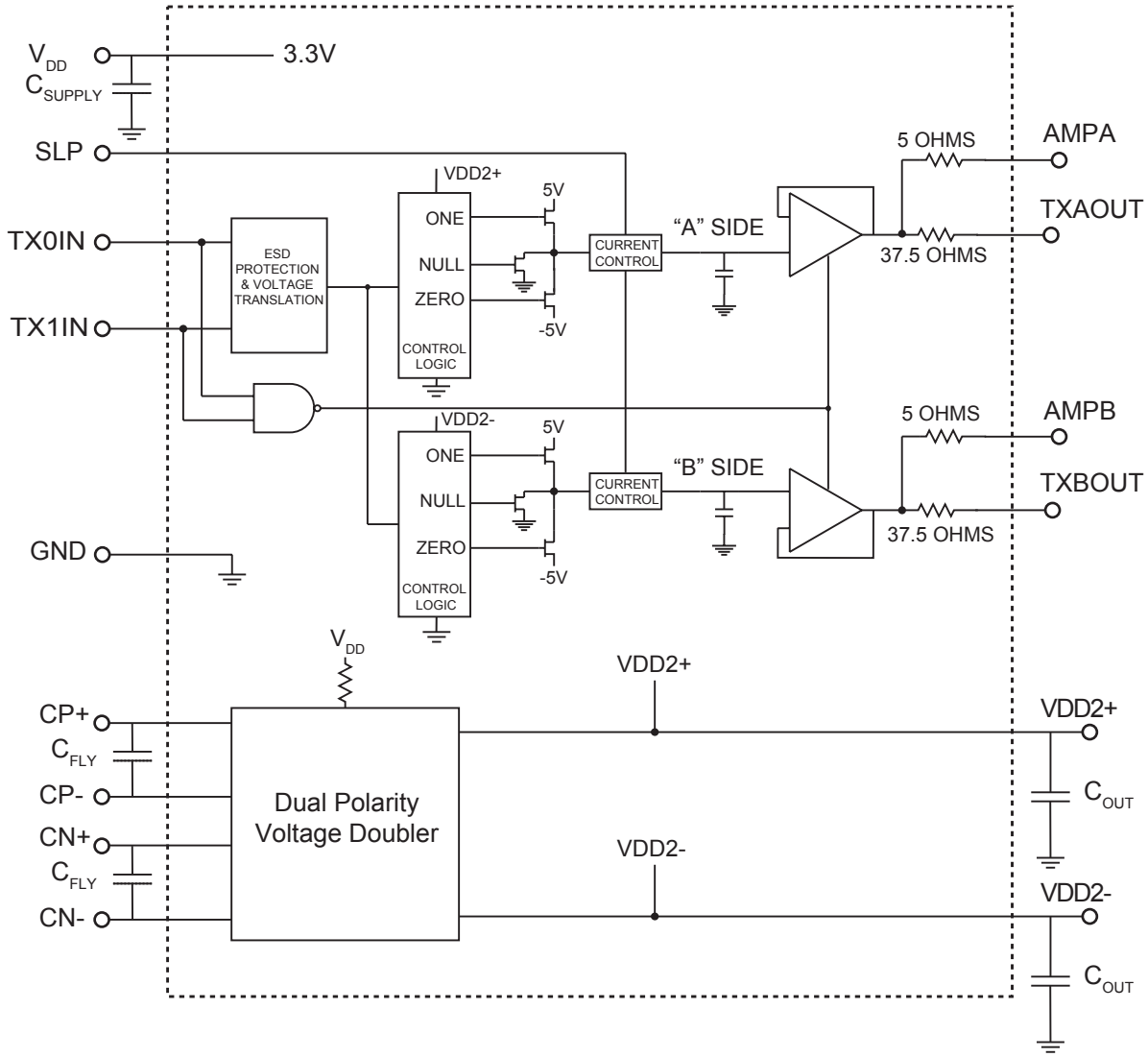


Figure 1. HI-8596 Block Diagram

PIN DESCRIPTIONS

Table 2. Pin Descriptions

Pin	Function	Description
SLP	INPUT	Output slew rate control. High selects ARINC 429 high-speed. Low selects ARINC 429 low-speed.
TX0IN	INPUT	Data input zero
TX1IN	INPUT	Data input one
V_{DD}	POWER	+3.3V power supply
GND	POWER	Ground supply
V_{DD2+}	OUTPUT	Voltage doubler positive output (~6.6V for 3.3V supply)
CP+	ANALOG	V_{DD2+} flyback capacitor, C_{FLY}; positive terminal
CP-	ANALOG	V_{DD2+} flyback capacitor, C_{FLY}; negative terminal
V_{DD2-}	OUTPUT	Voltage doubler negative output (~ -6.6V for 3.3V supply)
CN+	ANALOG	V_{DD2-} flyback capacitor, C_{FLY}; positive terminal
CN-	ANALOG	V_{DD2-} flyback capacitor, C_{FLY}; negative terminal
TXAOUT	OUTPUT	ARINC high output with 37.5 Ohms series resistance
AMPA	OUTPUT	ARINC high output with 5 Ohms series resistance
TXBOUT	OUTPUT	ARINC low output with 37.5 Ohms series resistance
AMPB	OUTPUT	ARINC low output with 5 Ohms series resistance

FUNCTIONAL DESCRIPTION

Figure 1 is a block diagram of the line driver. The HI-8596 requires only a single +3.3V power supply. An integrated inverting / non-inverting voltage doubler generates the rail voltages (±6.6V) which are then used to produce the ±5V ARINC-429 output levels.

The internal dual polarity charge pump circuit requires four external capacitors, two for each polarity generated by the doubler. CP+ and CP- connect the external charge transfer or "fly" capacitor, C_{FLY}, to the positive portion of the doubler, resulting in twice V_{DD} at the V_{DD2+} pin. An output "hold" capacitor, C_{OUT}, is placed between V_{DD2+} and GND. C_{OUT} should be ten times the size of C_{FLY}. The inverting or negative portion of the converter works in a similar fashion, with C_{FLY} and C_{OUT} placed between CN+ / CN- and V_{DD2-} / GND respectively.

Currents for slope control are set by on-chip resistors.

The TX0IN and TX1IN inputs receive logic signals from a control transmitter chip such as the HI-3584. TXAOUT and TXBOUT hold each side of the ARINC bus at Ground until one of the inputs becomes a One. If for example TX1IN goes high, a charging path is enabled to 5V on an "A" side internal capacitor while the "B" side is enabled to -5V. The charging current is selected by the SLP pin. If the SLP pin is high, the capacitor is nominally charged from 10% to 90% in 1.5µs. If SLP is low, the rise and fall times are 10µs.

A unity gain buffer receives the internally generated slopes and differentially drives the ARINC line. Current is limited by the series output resistors at each pin. There are no fuses at the outputs of the HI-8596.

The HI-8596 has 37.5 ohms in series with each TXOUT output and 5 ohms in series with each AMP output. The AMP outputs are for applications where external series resistance is required, typically for lightning protection devices. Holt Application Note AN-300 describes suitable lightning protection schemes.

Tri-stateable outputs allow multiple line drivers to be connected to the same ARINC 429 bus. Setting TX1IN and TX0IN both to a logic "1" puts the outputs in the high-impedance state.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	
V_{DD}	+5V
Junction Temperature (T_{JMAX})	175°C
Solder Temperature (reflow)	260°C
Storage Temperature	-65°C to +150°C

Note: HEAT SINK on QFN PACKAGE

The HI-8596 driver is available in a small-footprint, thermally enhanced QFN (chip-scale) package. This package includes an electrically isolated metal heat sink located on the bottom surface of the device. This heat sink should be soldered down to the printed circuit board for optimum thermal dissipation.

RECOMMENDED OPERATING CONDITIONS

Supply Voltages	
V_{DD}	+3.0V to +3.6V
Temperature Range	
Industrial Screening	-40°C to +85°C
Hi-Temp Screening	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

ELECTRICAL CHARACTERISTICS

Table 3. DC Electrical Characteristics

V_{DD} = +3.3V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage (TX1IN, TX0IN, SLP)						
High	V_{IH}		2.0	-	-	V
Low	V_{IL}		-	-	$0.3V_{DD}$	V
Input Current (TX1IN, TX0IN, SLP)		(73kΩ Internal Pulldown)				
	I_{IH}	V_{IN} = 3.3V	-	45	-	µA
	I_{IL}	V_{IN} = 0V	-	-	-0.1	µA
ARINC Output Voltage (Differential)						
one	V_{DIFF1}	no load; TXAOUT - TXBOUT	9	10	11	V
zero	V_{DIFF0}	no load; TXAOUT - TXBOUT	-11	-10	-9	V
null	V_{DIFFN}	no load; TXAOUT - TXBOUT	-0.5	0	0.5	V
ARINC Output Voltage (Ref. to GND)						
one or zero	V_{DOUT}	no load & magnitude at pin	4.5	5.0	5.5	V
null	V_{NOUT}	no load	-0.25	0	0.25	V
Operating Supply Current		SLP = V_{DD}				
No load	I_{DDNL}	TX1IN & TX0IN = 0V	-	28	40	mA
Max. Load	I_{DDL}	100kHz, 400Ω load	-	65	-	mA
ARINC Outputs Shorted	I_{DDS}	See Note 1	-	165	-	mA
Power Dissipation in device[2]		SLP = V_{DD}				
No load	P_{DDNL}	TX1IN & TX0IN = 0V	-	93	132	mW
Max. Load (AMPA to AMPB)	P_{DDLA}	100kHz, 400Ω load [3]	-	186	-	mW
Max. Load (TXAOUT to TXBOUT)	P_{DDLT}	100kHz, 400Ω load	-	215	-	mW
ARINC Outputs Shorted (AMP outputs)	P_{DDSA}	See Note 1	-	304	-	mW
ARINC Outputs Shorted (TXOUT outputs)	P_{DDST}	See Note 1		445	-	mW
ARINC Output Impedance	Z_{OUT}					
TXOUT pins				37.5		Ohms
AMP pins				5		Ohms
ARINC Output Tri-State Current	I_{OZ}	TX0IN = TX1IN = V_{DD} -5.75V < V_{OUT} < +5.75V	-1.0	0	+1.0	µA
ARINC Output Tri-State Voltage	V_{OZ}	TX0IN = TX1IN = V_{DD} -1.0µA < I_{OUT} < +1.0µA	-5.75	-	+5.75	V

Note 1: TXAOUT and/or TXBOUT shorted to each other or ground. AMPA and/or AMPB shorted to each other or ground (assumes external resistors are connected to AMPA and AMPB to comply with ARINC 429 37.5 Ohm output resistance requirement).

Note 2: Estimate junction temperature using Theta JB or Theta JA values available on Holt's website, www.holtic.com. $T_J \leq T_{JMAX}$.

Note 3: In addition, external resistors are connected to AMPA and AMPB to comply with ARINC 429 37.5 Ohm output resistance requirement

Table 4. Converter Characteristics

V_{DD} = +3.3V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Start-up transient (V+, V-)	t_{START}		-	-	10	ms
Operating Switching Frequency	f_{sw}		-	650	-	kHz
Worst case maximum voltage doubler output	$V_{DD2+(max)}$	V_{DD} = 3.6V. T = -55ºC. Open load.			6.93	V
DC/DC convertor capacitor recommendations. **For optimum performance use typical (not min.) values. For EMC compliance, see AN-135.**						
Ratio of bulk storage to fly-back capacitors	C_{OUT} / C_{FLY}		2.2	10		
Fly-back capacitor (Recommend ceramic, preferably multilayer, dielectric XR7 caps, 10V min.).	C_{FLY} $C_{FLY(ESR)}$	C_{OUT} / C_{FLY} >= 10 [0.5, 1.0]Mhz	1.0	4.7	- 500	µF mΩ
Bulk storage capacitor (Recommend ceramic, preferably multilayer, dielectric XR7 caps, 10V min.).	C_{OUT} $C_{OUT(ESR)}$	C_{OUT} / C_{FLY} >= 10 [0.5, 1.0]Mhz	2.2	47	- 300	µF mΩ
By-pass capacitor (Recommend ceramic cap, 10V min.).	C_{SUPPLY}	C_{SUPPLY} >= C_{OUT} (connect from V_{DD} to GND)				

Table 5. AC Electrical Characteristics

V_{DD} = +3.3V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Line Driver Propogation Delay		defined in Figure 2, no load				
Output high to low	t_{phlx}		-	500	-	ns
Output low to high	t_{plhx}		-	500	-	ns
Line Driver Transition Times						
High Speed		SLP = V_{DD}				
Output high to low	t_{fx}		1.0	1.5	2.0	µs
Output low to high	t_{rx}		1.0	1.5	2.0	µs
Low Speed		SLP = GND				
Output high to low	t_{fx}		5.0	10.0	15.0	µs
Output low to high	t_{rx}		5.0	10.0	15.0	µs
Input Capacitance (Logic)[1]	C_{IN}		-	-	10	pF
Output Capacitance (Tri-state)[1]	C_{OUT}	TX0IN = TX1IN = V_{DD}	-	-	10	pF

Note 1: Guaranteed but not tested

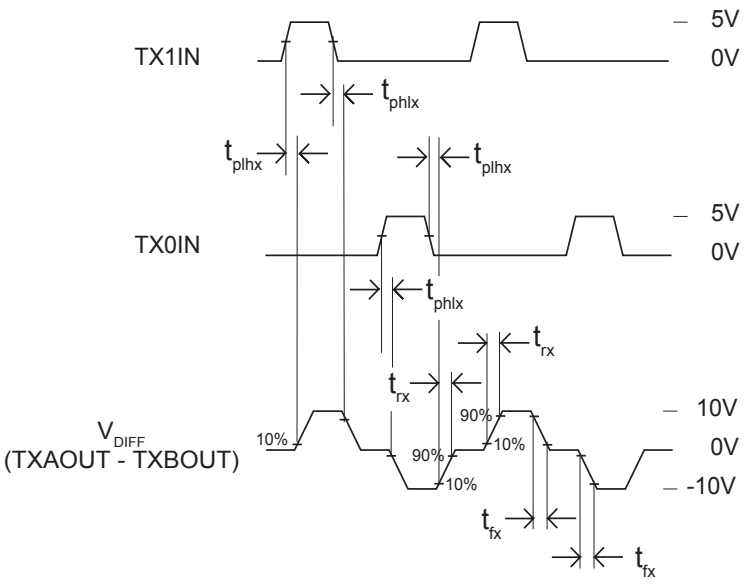


Figure 2. Line Driver Timing

ORDERING INFORMATION

HI - 8596PS x x (Plastic)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION	LEAD FINISH
8596PS	16 PIN PLASTIC SMALL OUTLINE - NB SOIC (16HN)	Solder

HI - 8596PC x x (Plastic)

PART NUMBER	LEAD FINISH
Blank	NiPdAu
F	NiPdAu (Pb-free RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION	LEAD FINISH
8596PC	16 PIN PLASTIC QFN (16PCS)	Solder

ORDERING INFORMATION (CONT.)

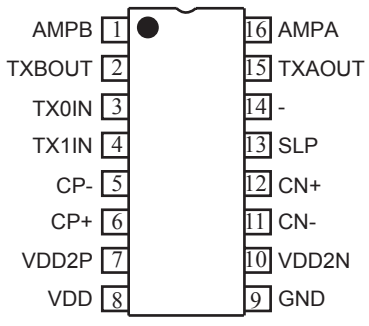
HI - 8596CD x (Ceramic)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
I	-40°C to +85°C	I	No	Gold (Pb-free, RoHS compliant)
T	-55°C to +125°C	T	No	Gold (Pb-free, RoHS compliant)
M	-55°C to +125°C	M	Yes	Tin / Lead (Sn / Pb) Solder

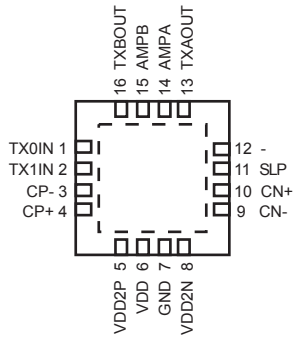
PART NUMBER	PACKAGE DESCRIPTION
8596CD	16 PIN CERAMIC SIDE BRAISED DIP (16C)

ADDITIONAL PIN CONFIGURATIONS

NOTE: All power and ground pins must be connected.



HI-8596CD
16-PIN CERAMIC SIDE-BRAZED DIP



HI-8596PC
16-LEAD 4mm x 4mm QFN

REVISION HISTORY

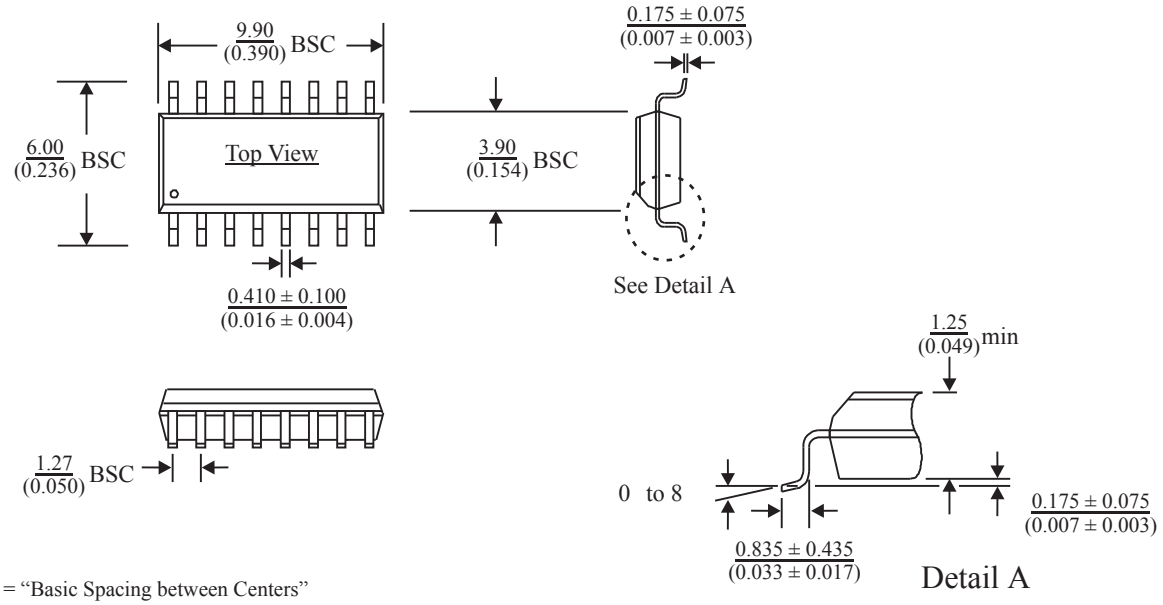
Revision	Date	Description of Change
DS8596, Rev. NEW	11/10/10	Initial Release
Rev. A	11/11/10	Clarified connection of heat sink and updated some electrical parameters (V_{IH}, V_{IL}, f_{sw}). Added operating supply current at full load (I_{DDL}).
Rev. B	7/14/11	Updated supply voltage range. Corrected dimensions on QFN heat sink. Added voltage limits for Tri-state output current.
Rev. C	5/21/12	Update DC/DC converter capacitor requirements in Table 4. Add spec for maximum tri-state output voltage.
Rev. D	11/9/12	Clarify DC/DC converter capacitor requirements in Table 4. Updated Solder Temperature (reflow) to 260°C. Added ARINC output short-circuit current.
Rev. E	12/11/12	Clarify operating supply current for shorted ARINC outputs.
Rev. F	01/27/14	Update SOIC-16 and QFN-16 package drawings.
Rev. G	07/24/14	Correct converter caps ESR values to be maximum instead of minimum.
Rev. H	01/08/15	Delete Max. Power Dissipation in Absolute Maximum Ratings table. Add Max. Junction Temperature to table. Add Device Power Dissipation to DC Electrical Characteristics in Table 3. Recommend ceramic converter caps only (no tantalum) in “Converter Characteristics”. Correct typo in ceramic DIP package ordering info. Update QFN package description from PCS1 to PCS.
Rev. I	07/22/15	Clarify Load condition for Power Dissipation in DC Electrical Characteristics in Table 3.
Rev. J	07/29/16	“Table 3. DC Electrical Characteristics”: change V_{IH} to 2.0V min. Correct input current pull down from 7.34 kΩ to 73 kΩ.
Rev. K	09/02/2021	Correct typo on SLP pin polarity for High Speed / Low Speed in “Table 5. AC Electrical Characteristics”.
Rev. L	07/07/2022	Clarify test conditions for I_{IH} and I_{IL} parameters.
Rev. M	11/30/2023	Clarify Input Current values on TX1IN, TX0IN and SLP pins.
Rev. N	06/12/2024	Update QFN package lead finish to NiPdAu.

PACKAGE DIMENSIONS

16-PIN PLASTIC SMALL OUTLINE (SOIC) - NB
(Narrow Body)

millimeters (inches)

Package Type: 16HN

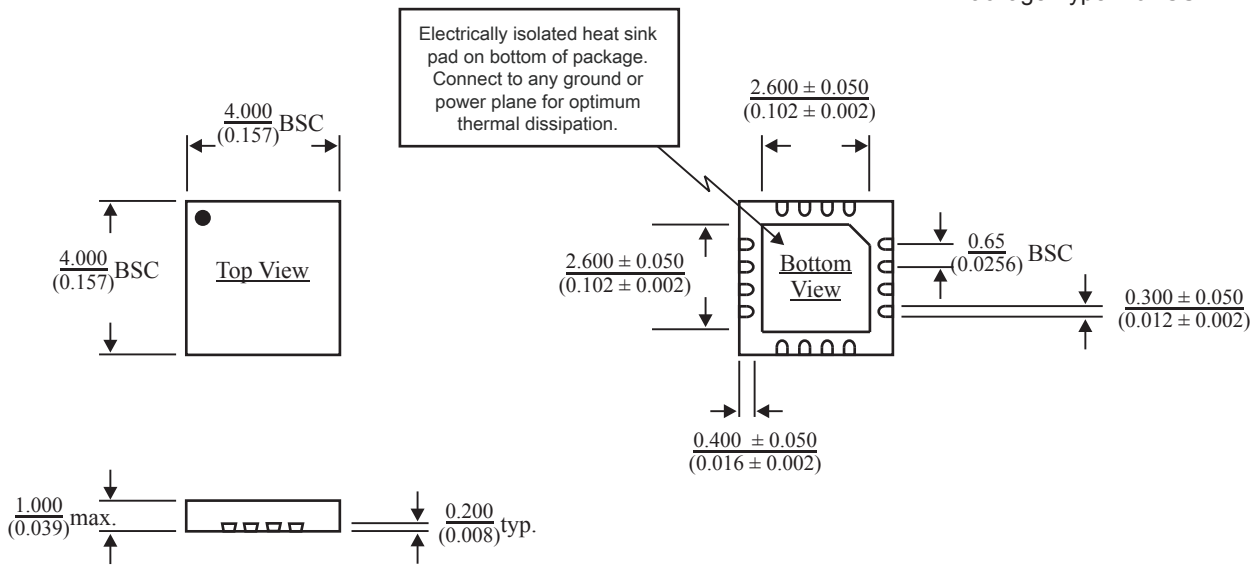


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

16-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 16PCS

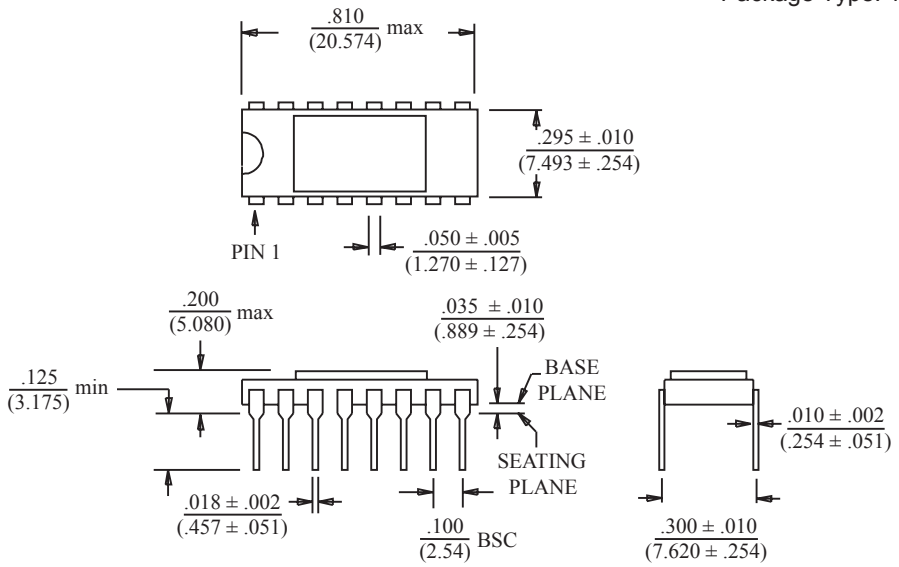


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

16-PIN CERAMIC SIDE-BRAZED DIP

inches (millimeters)

Package Type: 16C



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